

01 CHIP-LEVEL COMPARISON

HF Card Inlay

Technical reference

Six 13.56 MHz chip references for comparing interface, memory and intended use. This is a reference document, not a list of currently available RFIDAK configurations.

Chip / source	Reader interface	Memory area	Typical application
NTAG213 [1]	ISO/IEC 14443 Type A · NFC Forum Type 2	144 bytes user memory	NFC cards carrying a short web link or text record.
NTAG215 [1]	ISO/IEC 14443 Type A · NFC Forum Type 2	504 bytes user memory	NFC cards carrying a larger record or several small records.
NTAG216 [1]	ISO/IEC 14443 Type A · NFC Forum Type 2	888 bytes user memory	NFC cards with more information stored directly on the chip.
MIFARE DESFire EV3 [2]	ISO/IEC 14443 Type A, Parts 1-4 · NFC Forum Type 4	2 / 4 / 8 / 16 kB non-volatile memory Capacity depends on the IC variant; files and application structure use this memory.	Access and multi-application credentials using a DESFire application.
MIFARE Classic EV1 1K [3]	ISO/IEC 14443 Type A activation · MIFARE Classic commands	1 kB total EEPROM · 16 sectors Includes manufacturer data and sector trailers; 1 kB is not all application space.	Existing card systems designed for MIFARE Classic 1K.
ICODE SLIX2 [4]	ISO/IEC 15693	316 bytes user data · separate counter block 80 × 4-byte blocks: 79 for user data and the final block for the counter function.	ISO/IEC 15693 cards for library, asset and document systems.

Read memory figures correctly. Memory figures describe different areas of each chip. NDEF formatting, application files and access-control data use part of the available space. NTAG user memory is a read/write area; NDEF formatting also occupies space.

Manufacturer references | Reviewed 2026-09-15

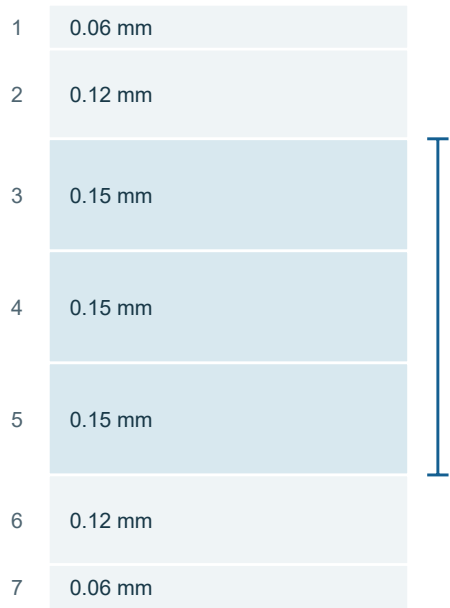
- [1] NXP: NTAG213_215_216, Rev. 3.2, 2 June 2015
- [2] NXP: MF3D(H)x3, Rev. 3.1, 11 January 2024
- [3] NXP: MF1S50YYX_V1, Rev. 3.2, 23 May 2018
- [4] NXP: SL2S2602, Rev. 4.2, 1 December 2021

02 HISTORICAL CONSTRUCTION EXAMPLE

What the layer thickness means

ACT Trinnovation 2017-Q4, slide 21. A 2017 reference drawing shows three 0.15 mm inlay layers within a seven-layer card. This describes the illustrated stack, not a current RFIDAK supply specification.

Schematic cross-section



Layer (front to reverse)

Layer (front to reverse)	mm
1. Front overlay	0.06
2. Front printing layer	0.12
3. Inlay top cover	0.15
4. Antenna core	0.15
5. Inlay bottom cover	0.15
6. Reverse printing layer	0.12
7. Reverse overlay	0.06

Blue layers: inlay subtotal. Thickness proportions are shown; there are no sheet, antenna or finished-card XY dimensions in this schematic.

0.45 mm

Three central inlay layers: 0.15 + 0.15 + 0.15

0.81 mm

Complete illustrated card stack

Full stack arithmetic: 0.06 + 0.12 + 0.15 + 0.15 + 0.15 + 0.12 + 0.06 = 0.81 mm.
The 0.45 mm inlay subtotal is calculated from the three central layers; the source drawing states a 0.81 mm complete card.

Source and scope

Redrawn from **ACT Trinnovation 2017-Q4 (ACT), slide 21**. The English layer labels aid reading of the historical example. It is not a current RFIDAK engineering drawing, supplier qualification or finished-card specification.

Use this reference when requesting an order specification

- Chip and supply.** These are NXP chip-level references. Your quotation identifies the supplied chip, sheet construction and production availability.
- Order drawing.** The selected model, sheet and antenna dimensions, stack thickness and tolerances belong in the order drawing.
- Commercial terms.** Your quotation sets quantities, sample scope, production lead time and delivery terms for that configuration.